FIG. 1.
(PRIOR ART)

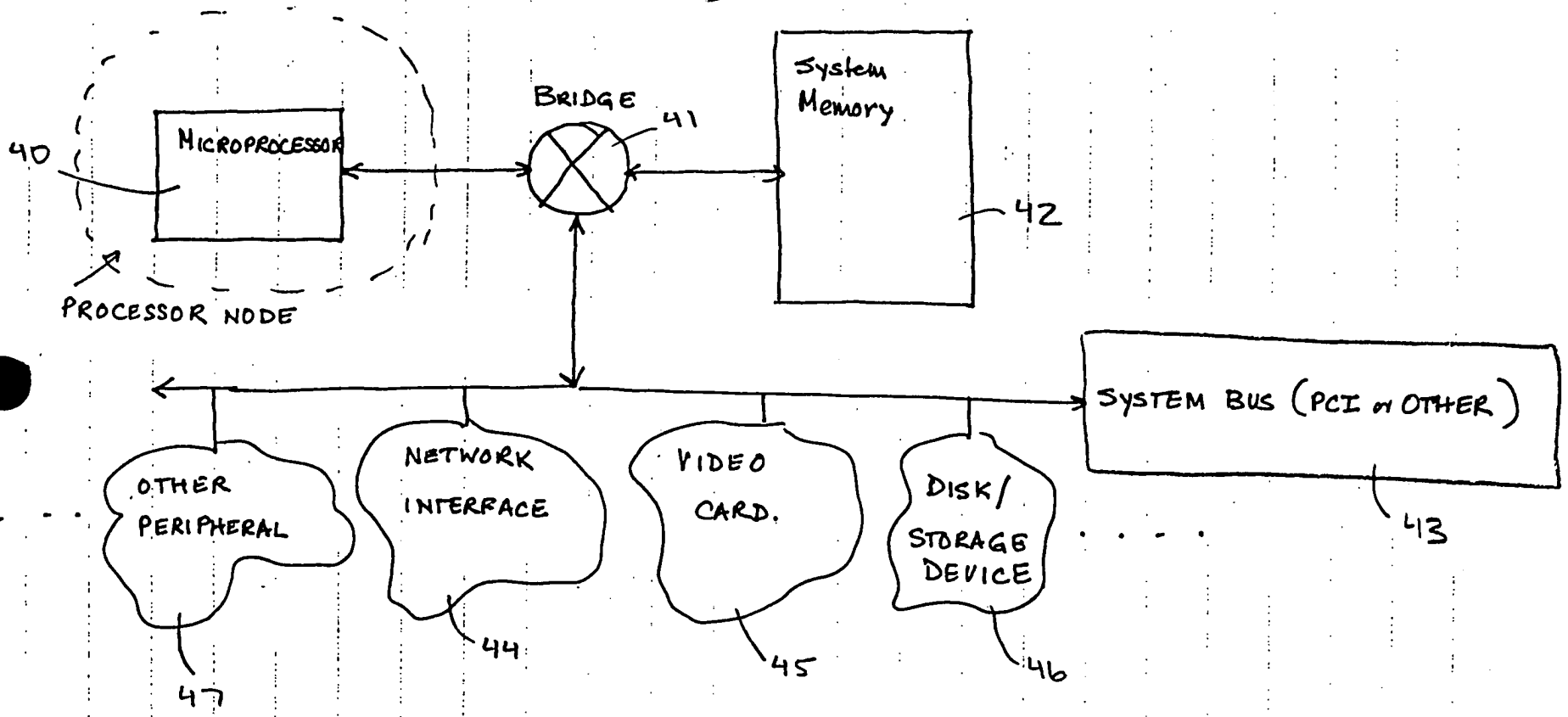

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FIG. 2.

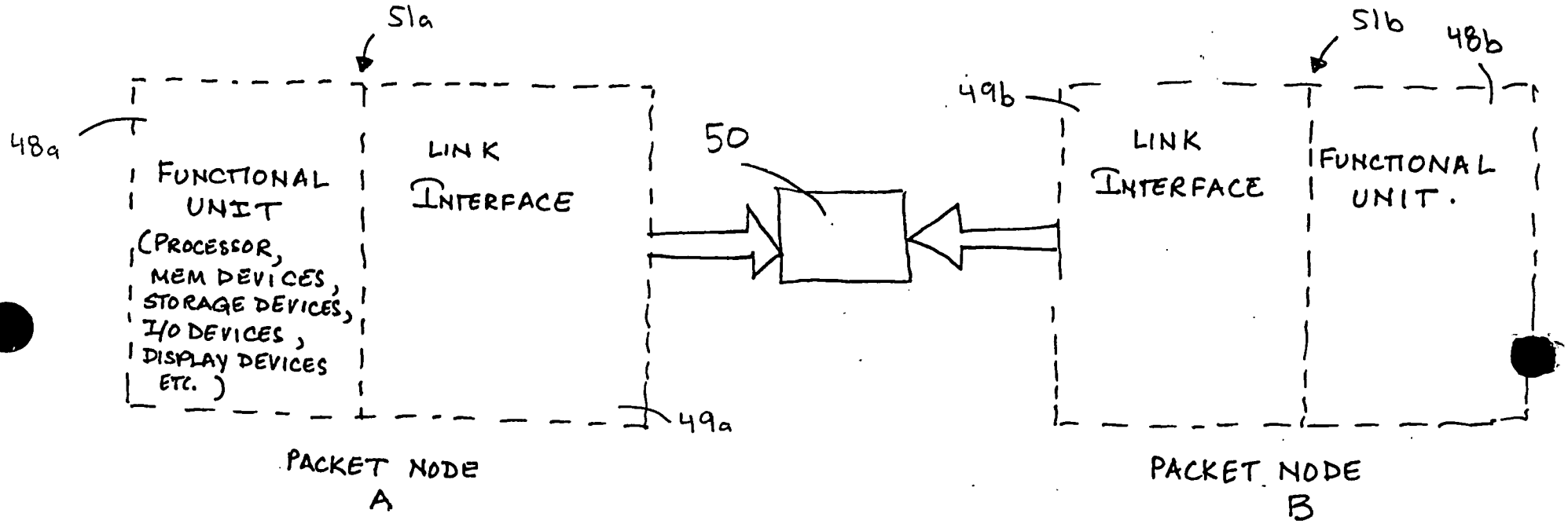
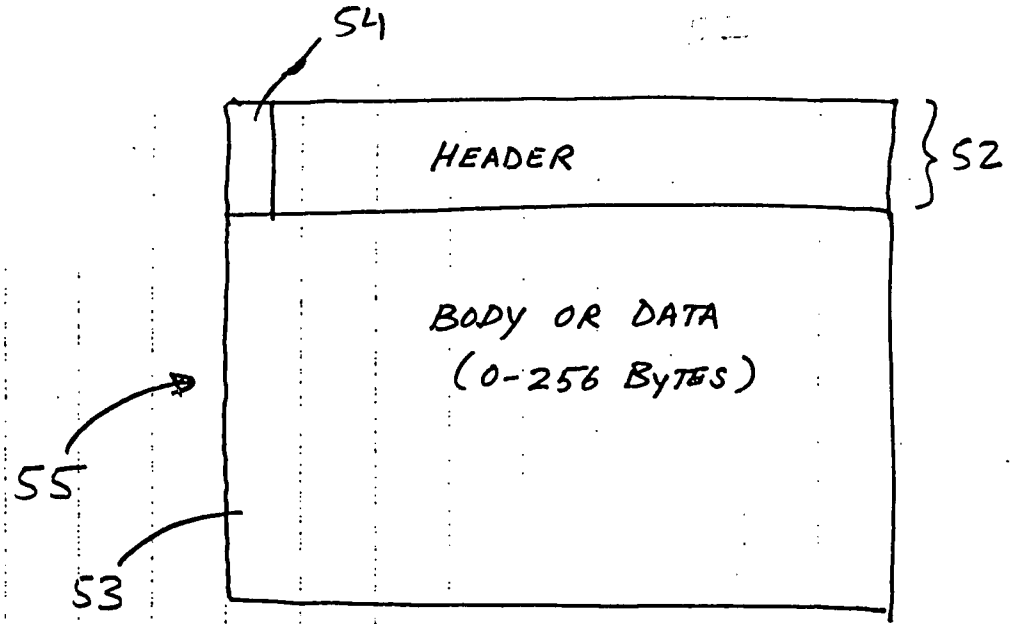

51a
48a
FUNCTIONAL UNIT
(PROCESSOR, MEM DEVICES, STORAGE DEVICES, I/O DEVICES, DISPLAY DEVICES ETC.)
LINK INTERFACE
50
49a
PACKET NODE A
51b
48b
49b
LINK INTERFACE
FUNCTIONAL UNIT.
PACKET NODE B

FIG. 3.



WIDTH = 2 BYTES

SIZE = 2 BYTES TO A MAXIMUM OF 258 BYTES.

2627575 "05/05/80

FIG. 4.

FIG 5.

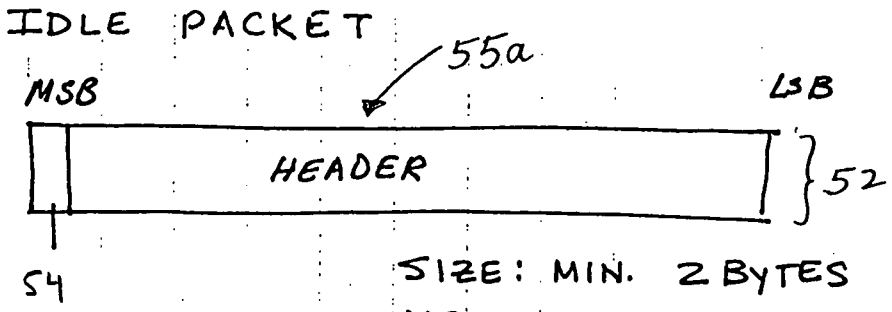


FIG. 6.

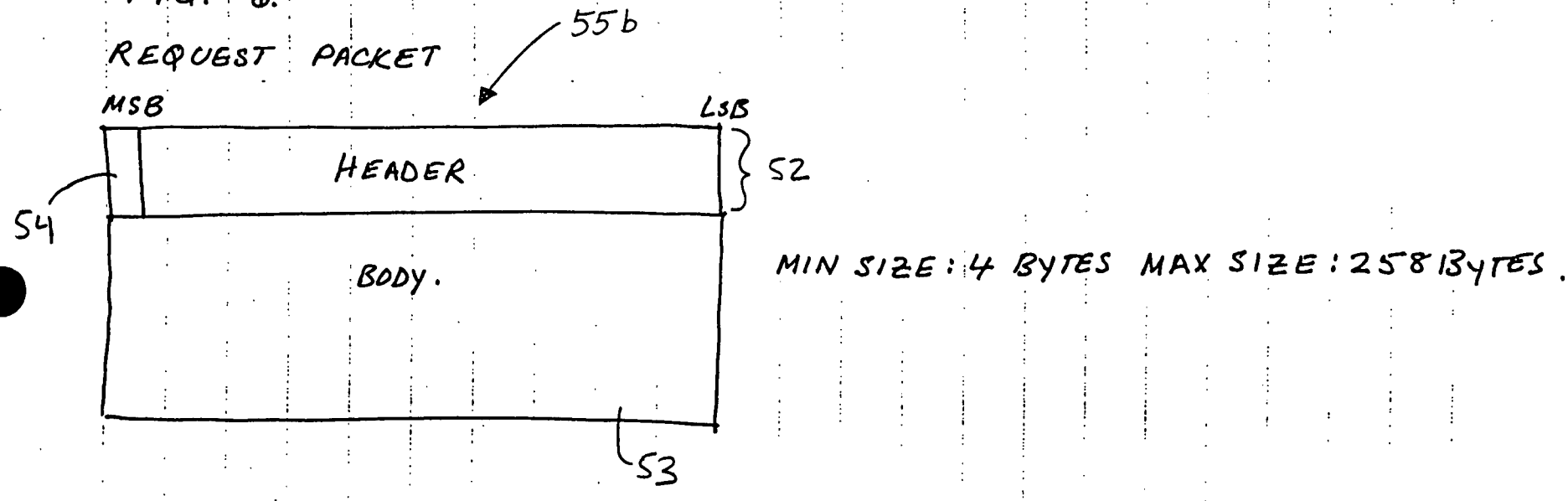


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FIG. 7.

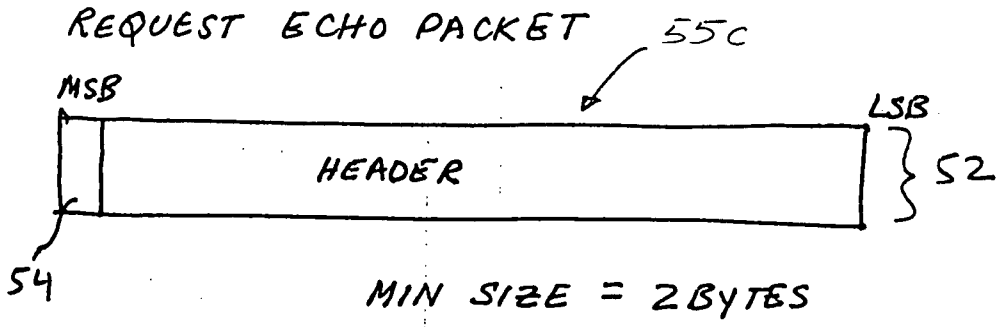

FIG. 8 RESPONSE PACKET

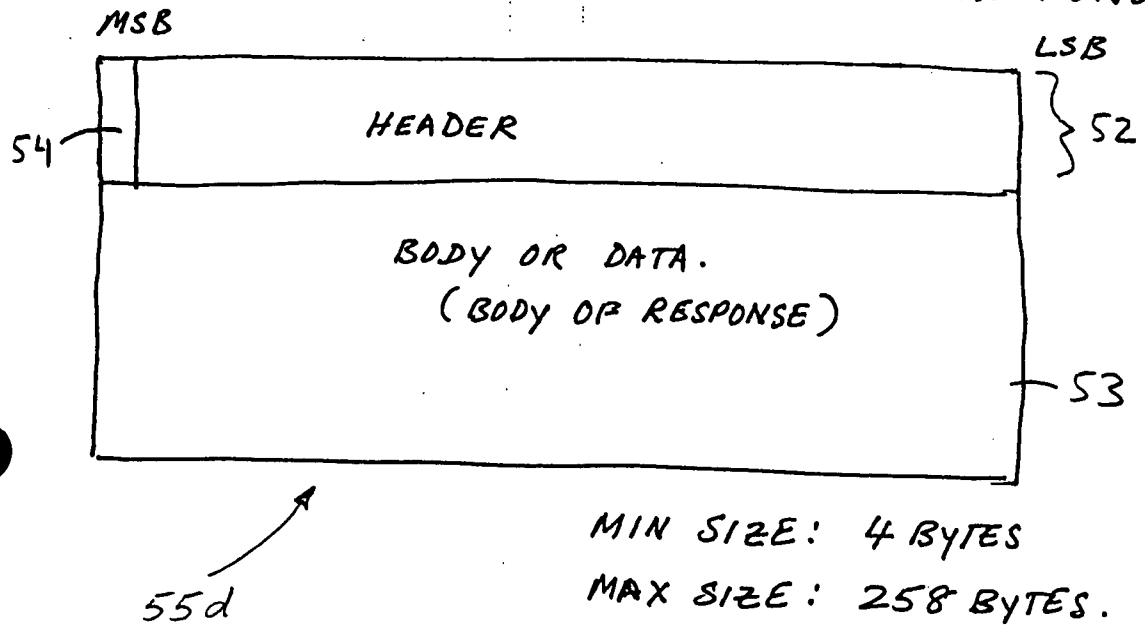

FIG. 9.

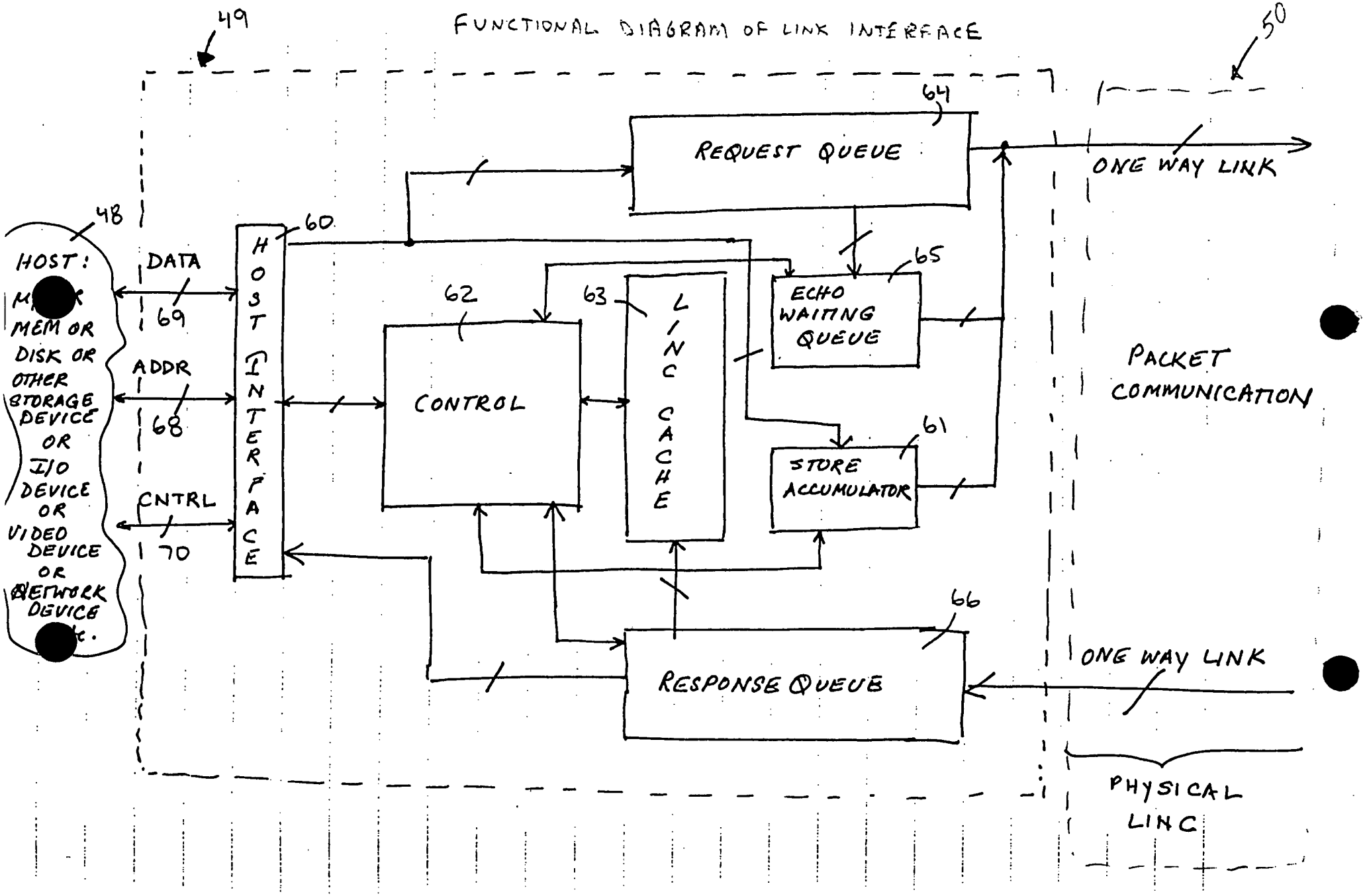

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FIG. 10

POSSIBLE REQUEST QUEUE STRUCTURES

FIG 10a.

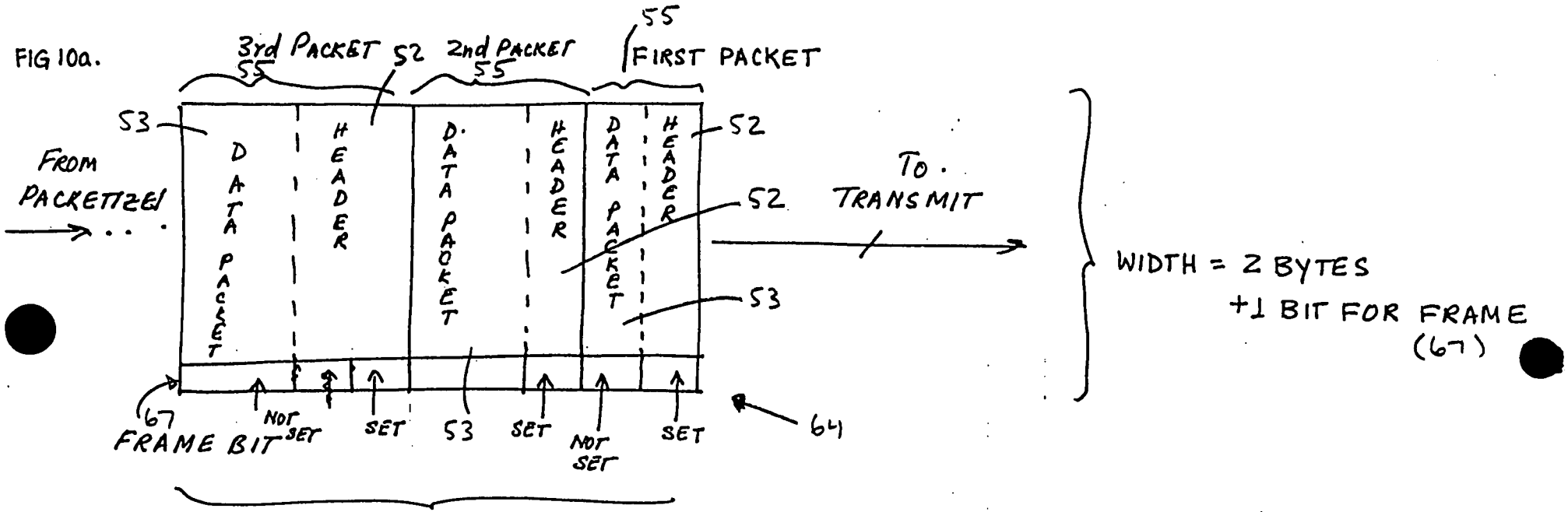

FIG. 10b.

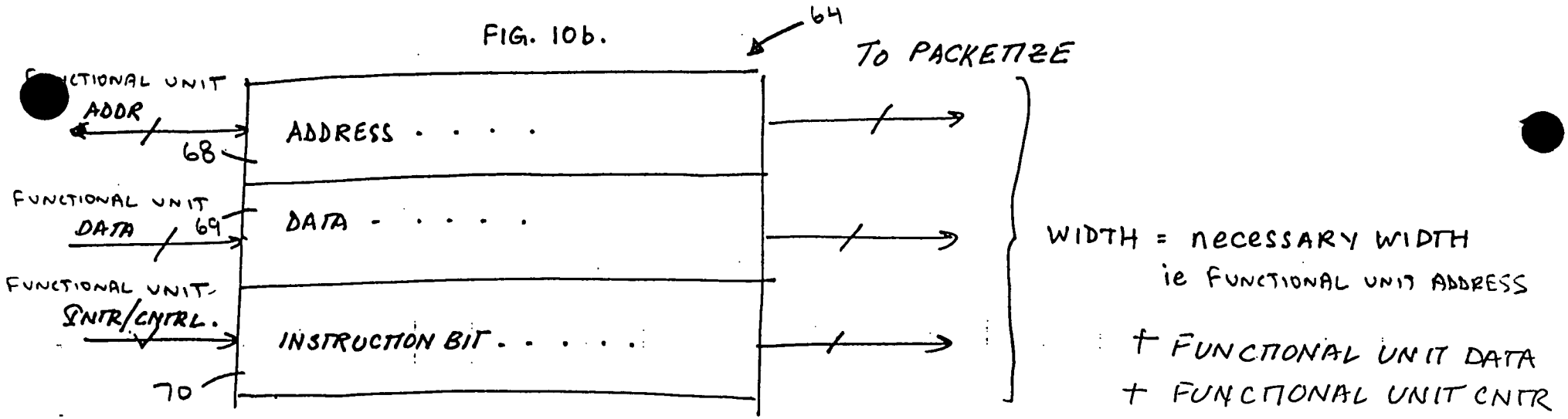

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FIG 11.

POSSIBLE RESPONSE QUEUE STRUCTURES.

FIG 11a.

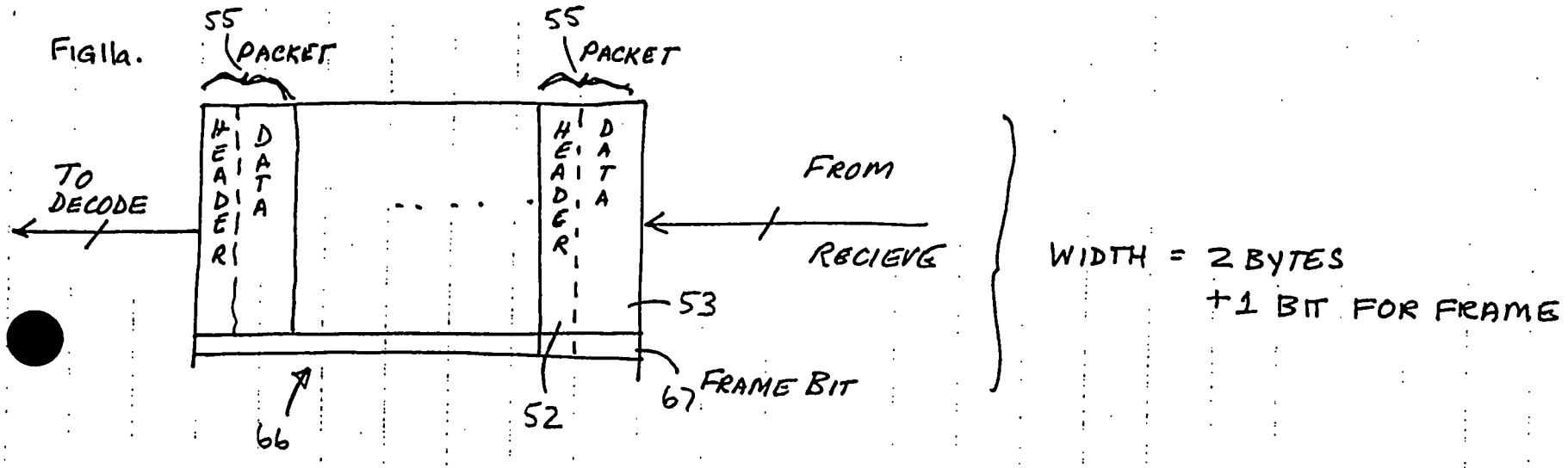

FIG 11b.

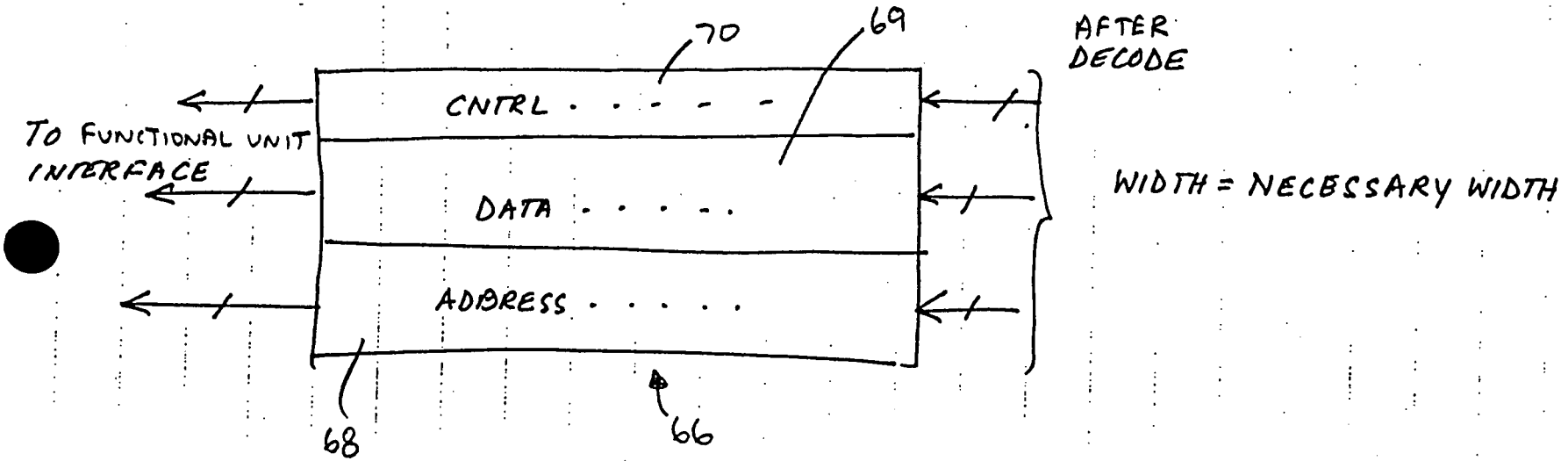

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FIG. 12.

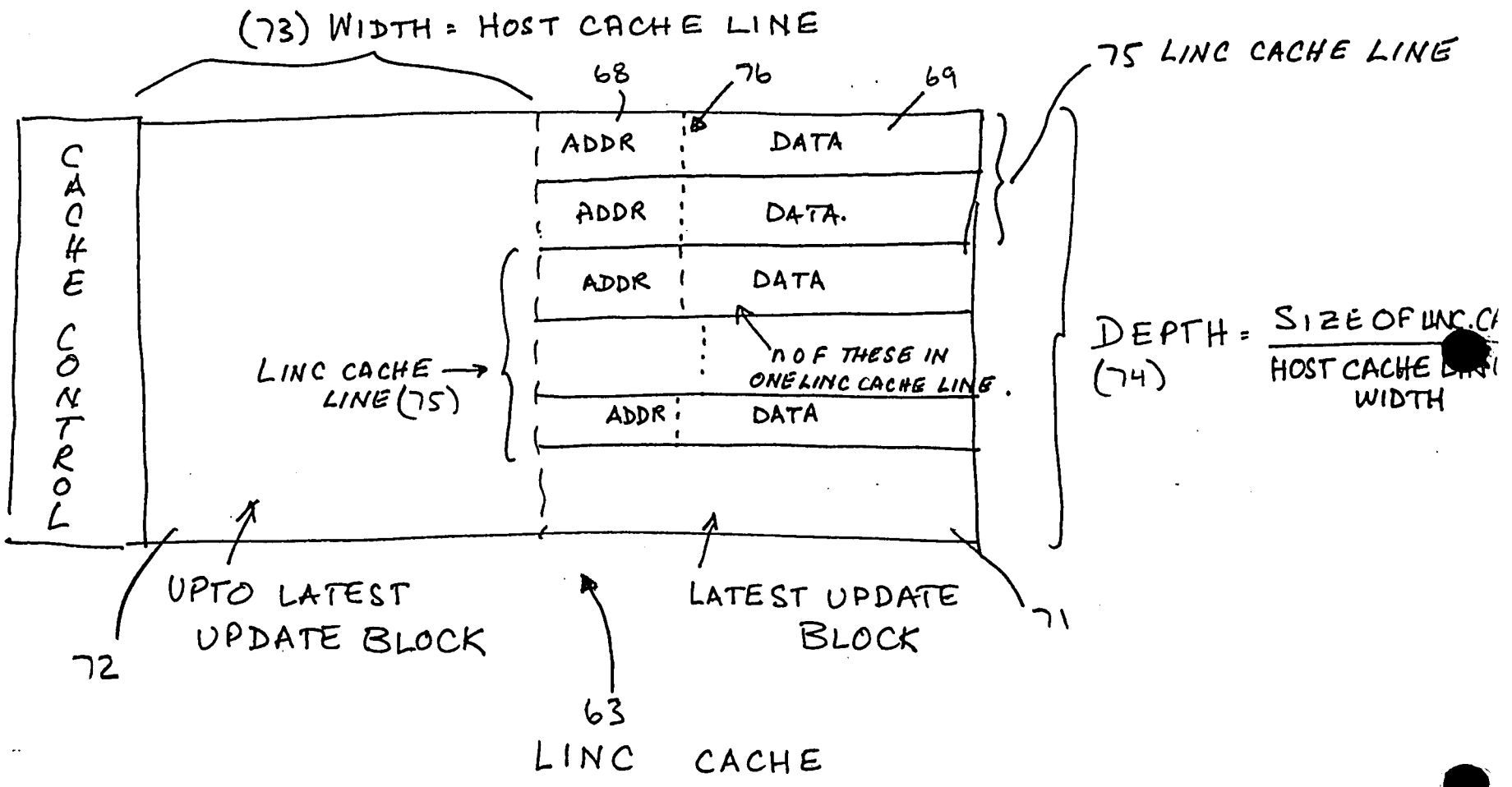

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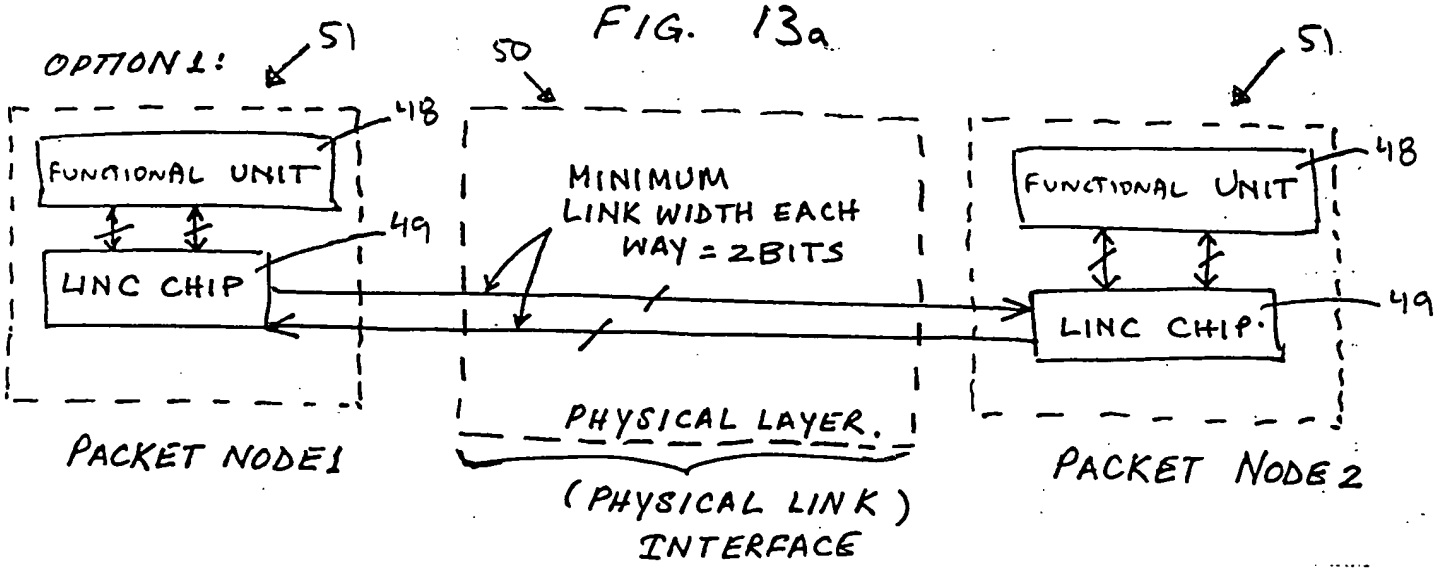
FIG. 13a



A SAMPLE TWO NODE LINK WHERE NODE1 FUNCTIONAL UNIT IS THE PROCESSOR AND NODE 2 FUNCTIONAL UNIT IS THE MEMORY.

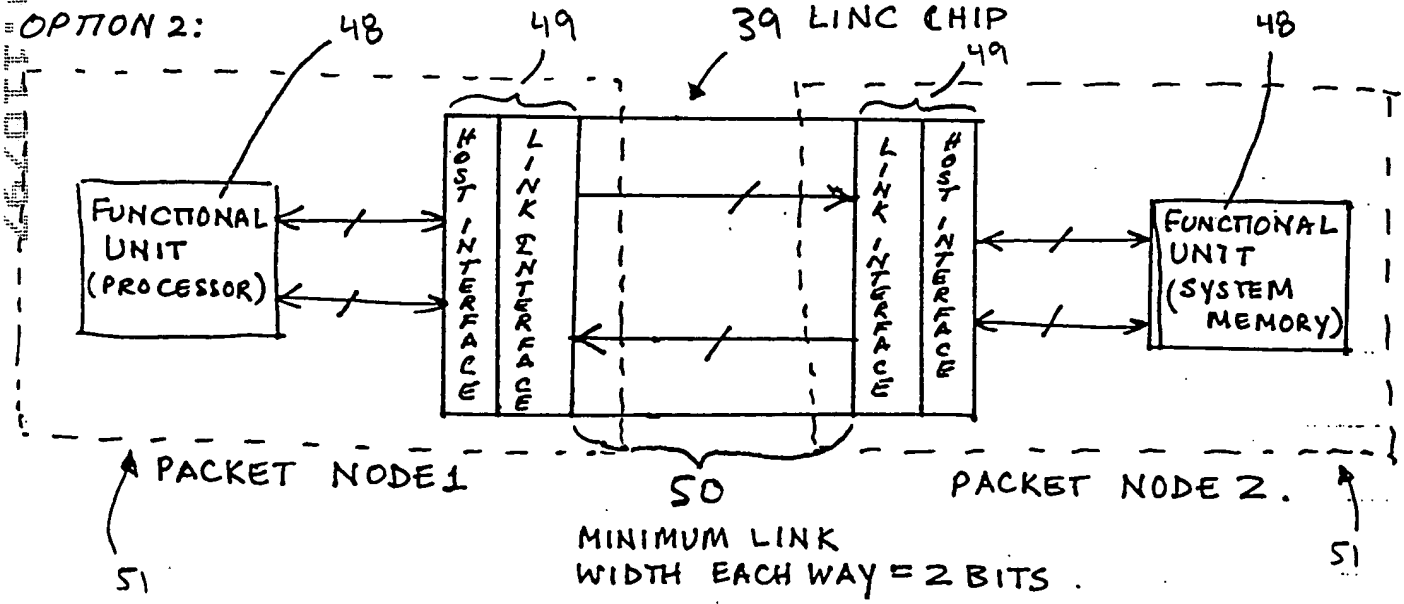


FIG. 13b

FIG. 14.

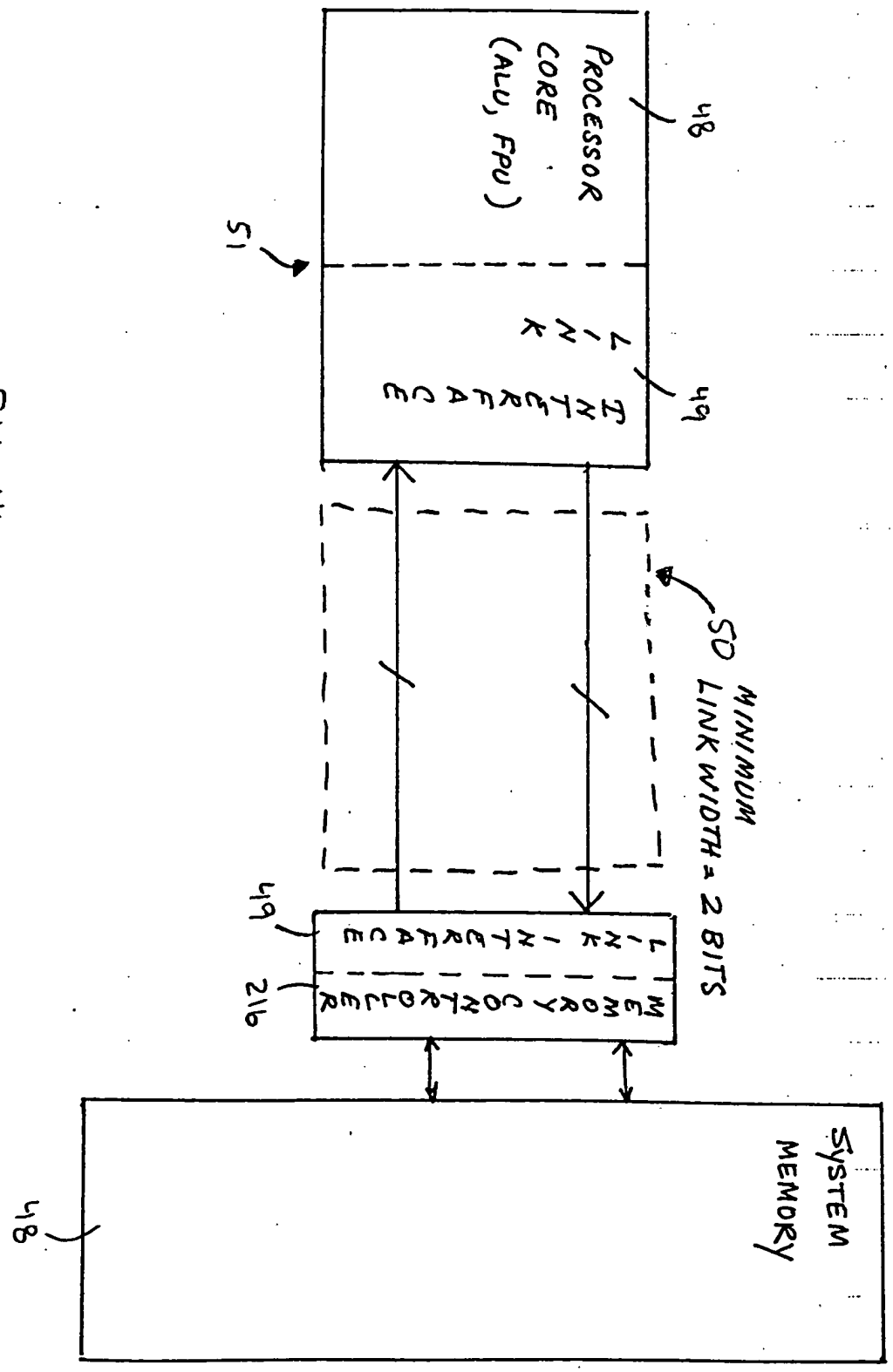

PROCESSOR CORE (ALU, FPU)
48
51
49
SD MINIMUM LINK WIDTH = 2 BITS
49
216
48
SYSTEM MEMORY

FIG. 14.

FIG. 15

IDLE PACKET:

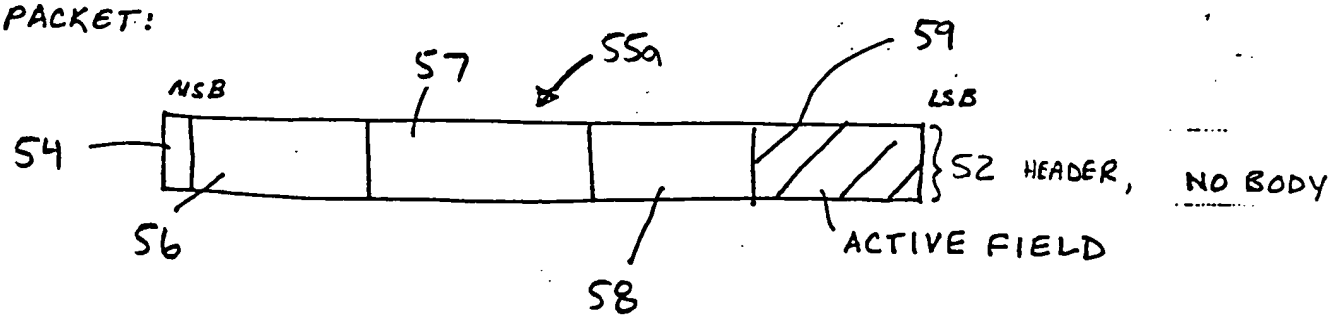


FIG. 16

REQUEST PACKET:

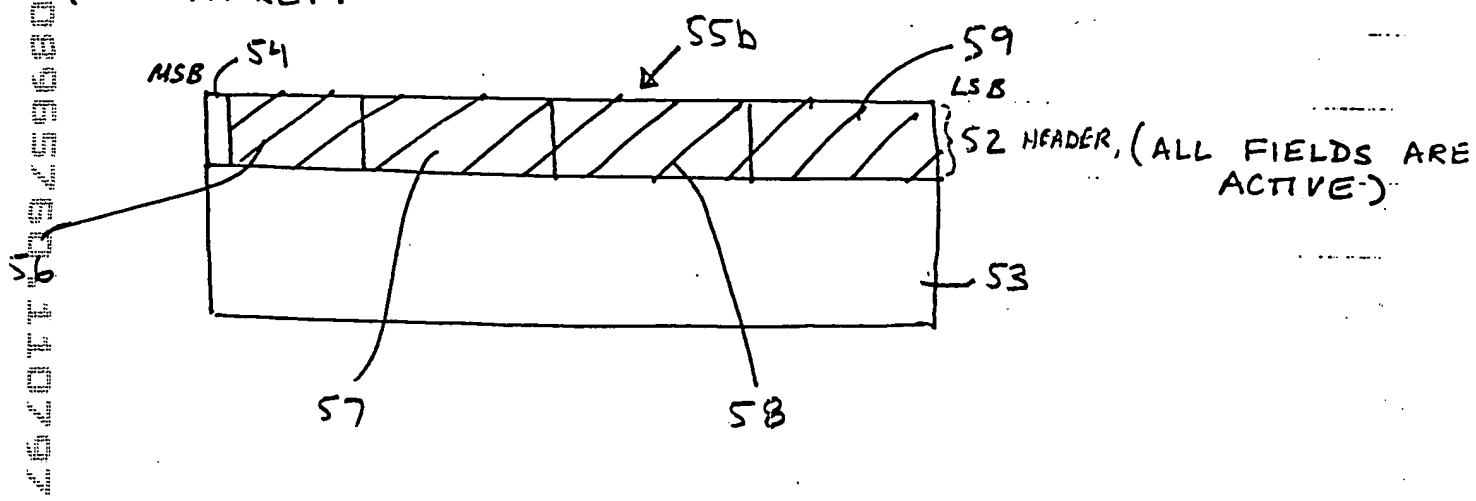


FIG. 17

REQUEST ECHO PACKET:

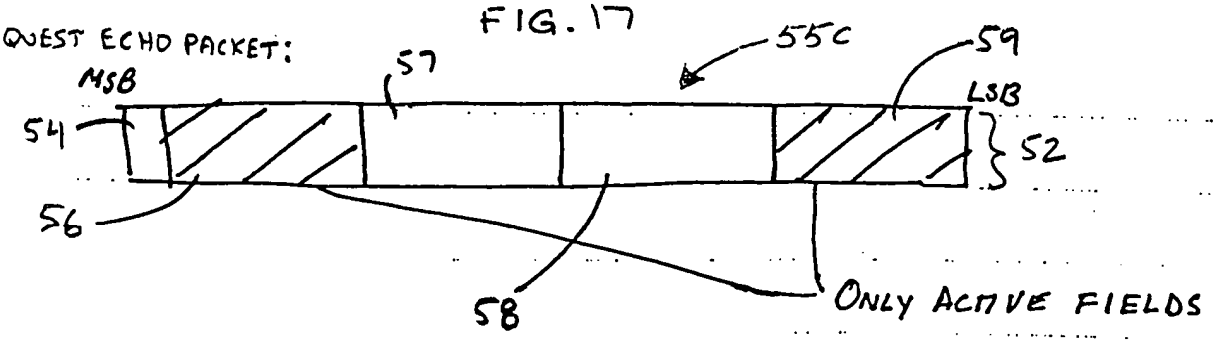


FIG. 18

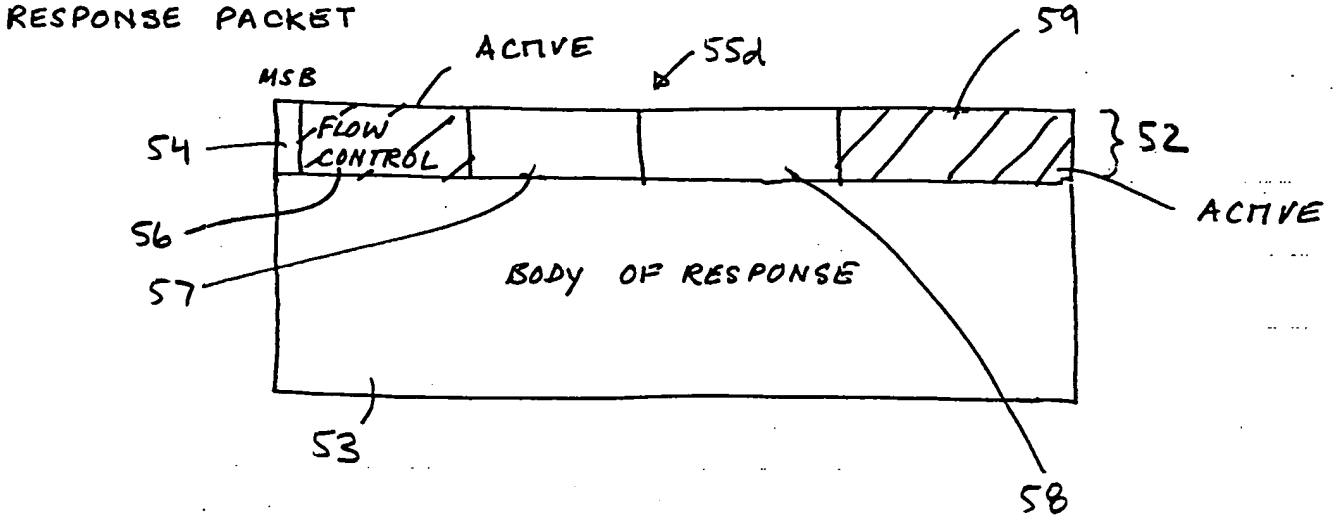
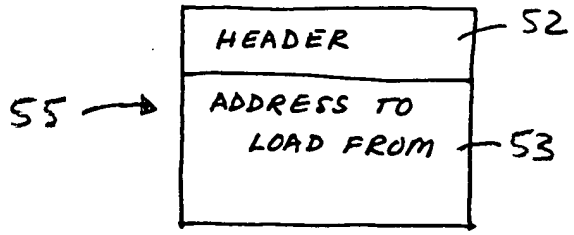
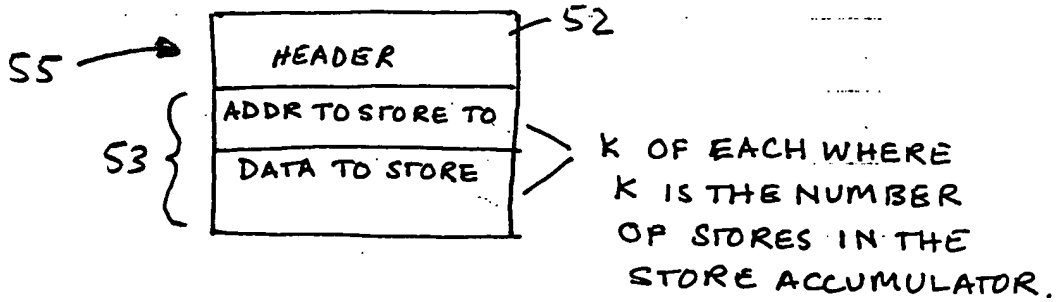


FIG. 19

REQUEST PACKET FOR A LOAD.



REQUEST PACKET FOR A STORE



Google-Exhibit-1005

FIG. 20

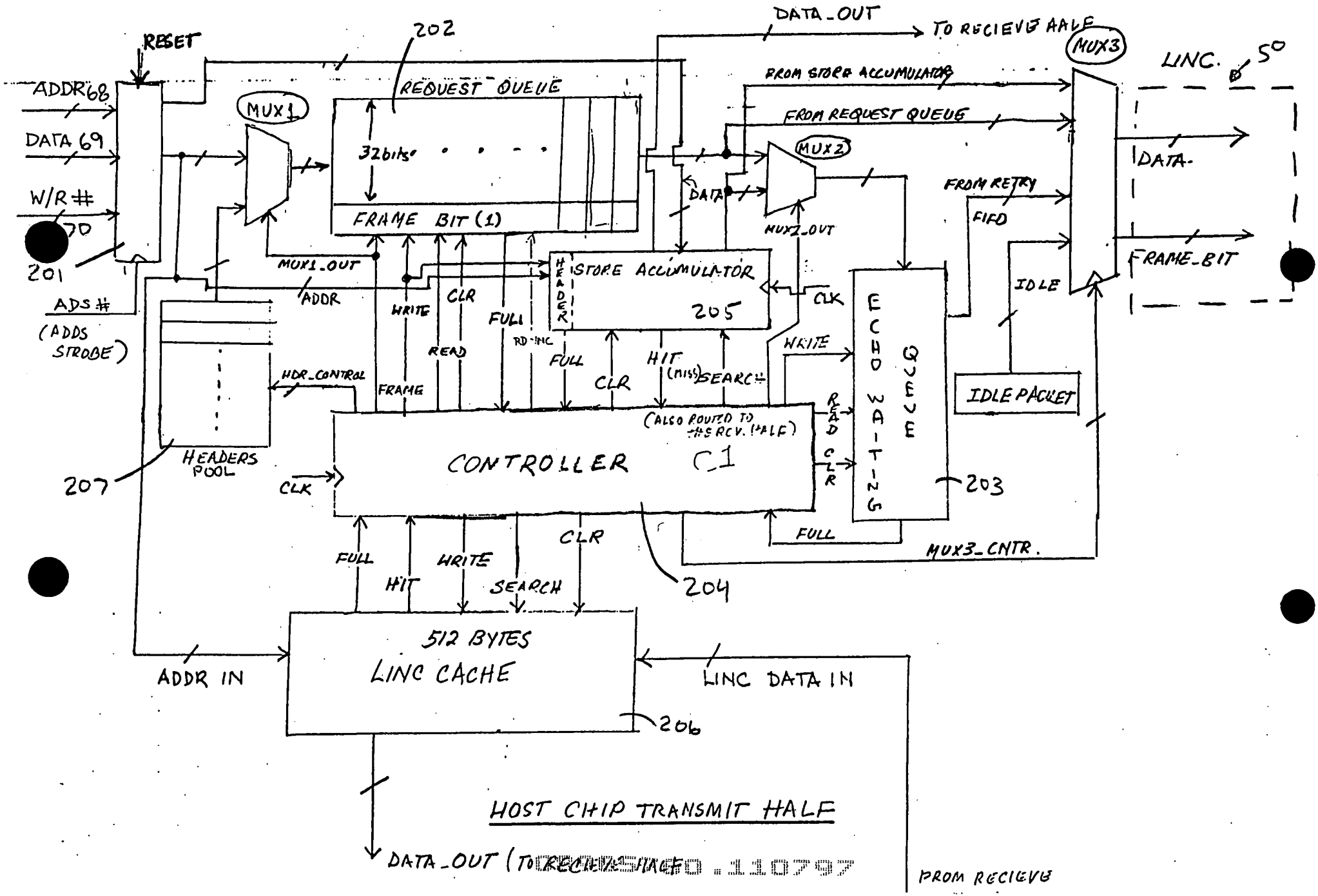
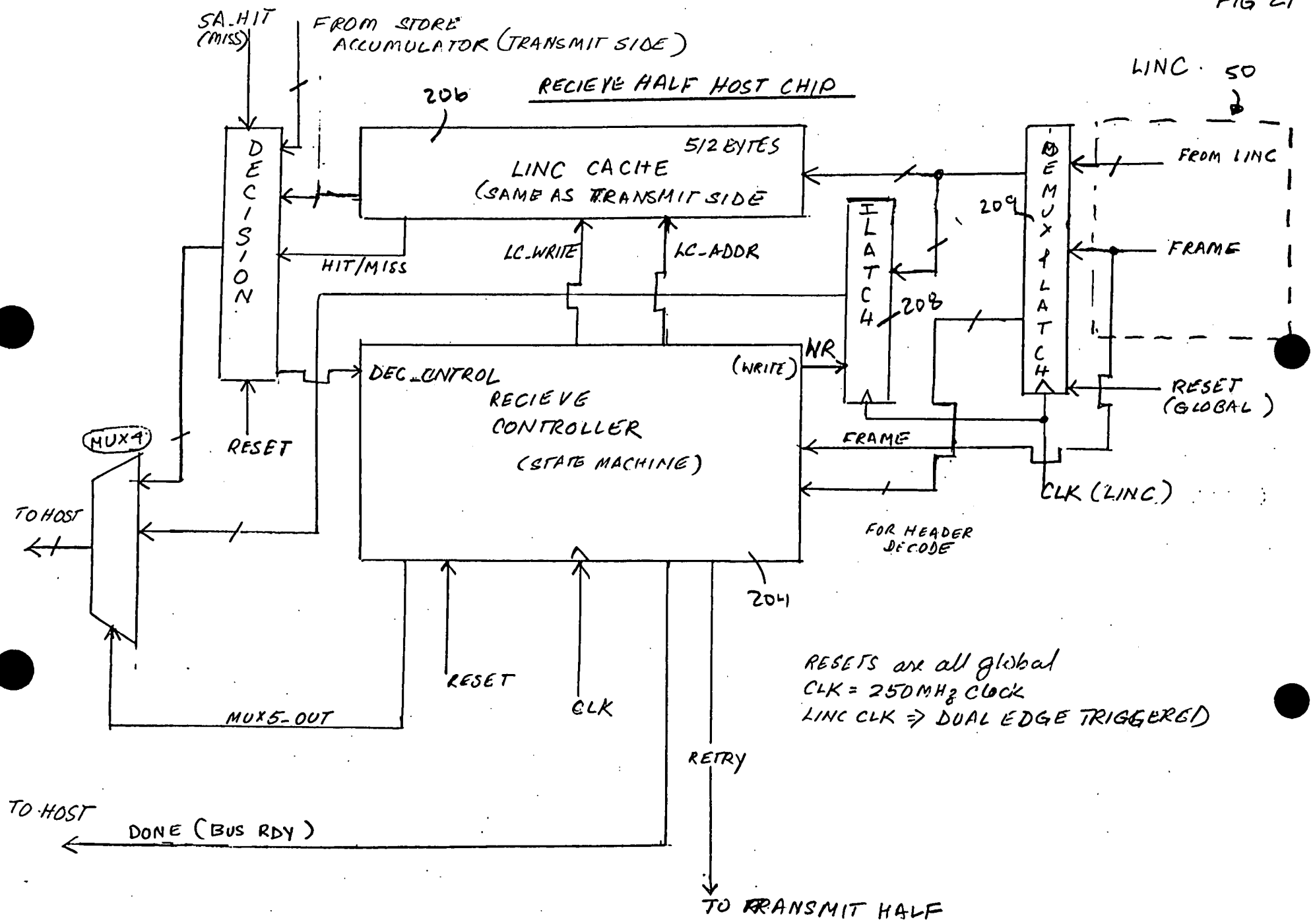

RESET
202
DATA_OUT
TO RECIEVE HALF
MUX3
LINC. 50
ADDR 68
DATA 69
W/R #
70
201
ADDS #
(ADDS STROBE)
MUX1
REQUEST QUEUE
32bits
FRAME BIT (1)
FROM STORE ACCUMULATOR
FROM REQUEST QUEUE
MUX2
DATA
MUX2_OUT
FROM RETRY FIFO
DATA
FRAME_BIT
MUX1_OUT
ADDR
STORE ACCUMULATOR
205
HEADER
WRITE
CLR
FULL
RD_INC
READ
FULL
CLR
HIT (MISS)
SEARCH
CLK
WRITE
IDLE
HDR_CONTROL
FRAME
(ALSO ROUTED TO HS RCV. HALF)
IDLE PACKET
HEADERS POOL
207
CONTROLLER C1
READ
CLR
ECHO WAITING QUEUE
203
CLK
FULL
MUX3_CNTR.
FULL
HIT
WRITE
SEARCH
CLR
204
512 BYTES
LINC CACHE
206
ADDR IN
LINC DATA IN
HOST CHIP TRANSMIT HALF
DATA_OUT (TO RECEIVE HALF)
FROM RECIEVE

FIG 21



RESETS are all global
CLK = 250MHz Clock
LINC CLK => DUAL EDGE TRIGGERED

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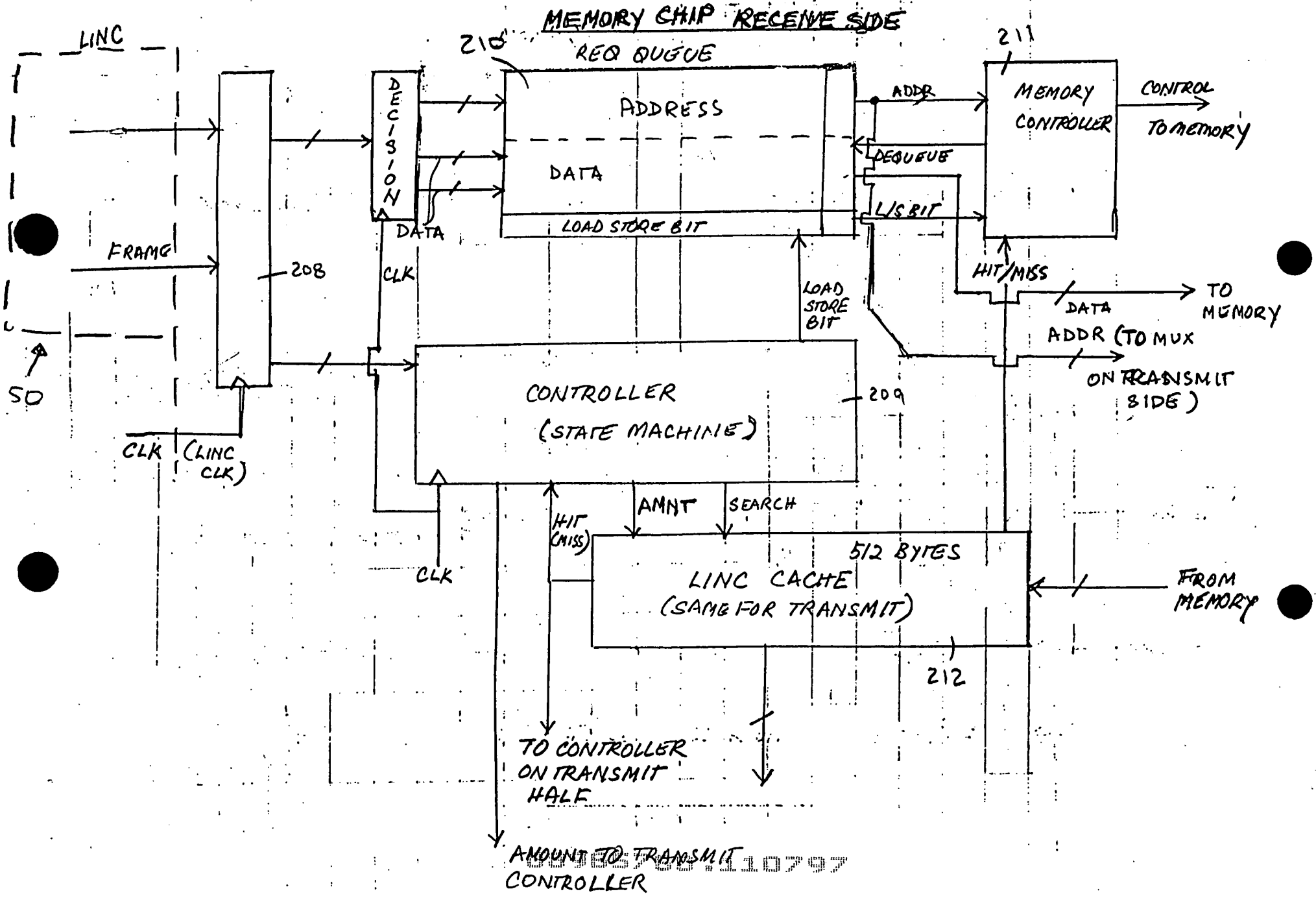
FIG. 22


MEMORY CHIP RECEIVE SIDE
LINC
210
REQ QUEUE
211
ADDRESS
DATA
LOAD STORE BIT
DECISION
DATA
ADDR
DEQUEUE
L/S BIT
MEMORY CONTROLLER
CONTROL TO MEMORY
HIT/MISS
DATA
TO MEMORY
ADDR (TO MUX ON TRANSMIT SIDE)
FRAME
208
CLK
SD
CLK (LINC CLK)
LOAD STORE BIT
CONTROLLER (STATE MACHINE)
209
AMNT
SEARCH
HIT (MISS)
512 BYTES
LINC CACHE (SAME FOR TRANSMIT)
FROM MEMORY
212
CLK
TO CONTROLLER ON TRANSMIT HALF
AMOUNT TO TRANSMIT CONTROLLER

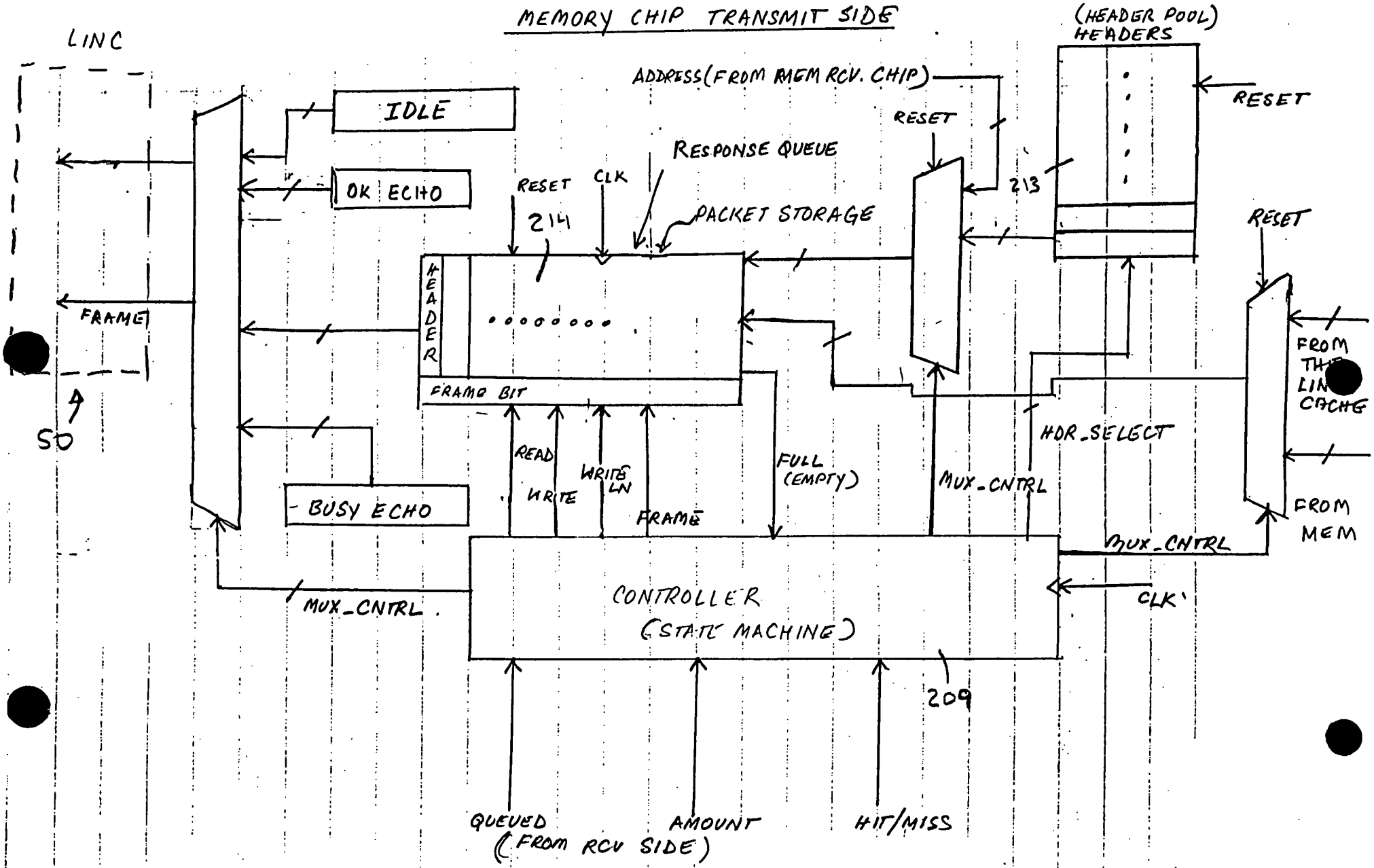

MEMORY CHIP TRANSMIT SIDE
LINC
(HEADER POOL)
HEADERS
ADDRESS(FROM MEM RCV. CHIP)
RESET
IDLE
OK ECHO
RESPONSE QUEUE
RESET
CLK
PACKET STORAGE
214
213
RESET
FRAME
HEADER
FRAME BIT
50
FROM THE LINC CACHE
HDR_SELECT
READ
WRITE
WRITE LN
FULL (EMPTY)
MUX_CNTRL
BUSY ECHO
FRAME
MUX_CNTRL
FROM MEM
CONTROLLER
(STATE MACHINE)
MUX_CNTRL
CLK
209
QUEUED
(FROM RCV SIDE)
AMOUNT
HIT/MISS

FIG. 23

FIG. 24

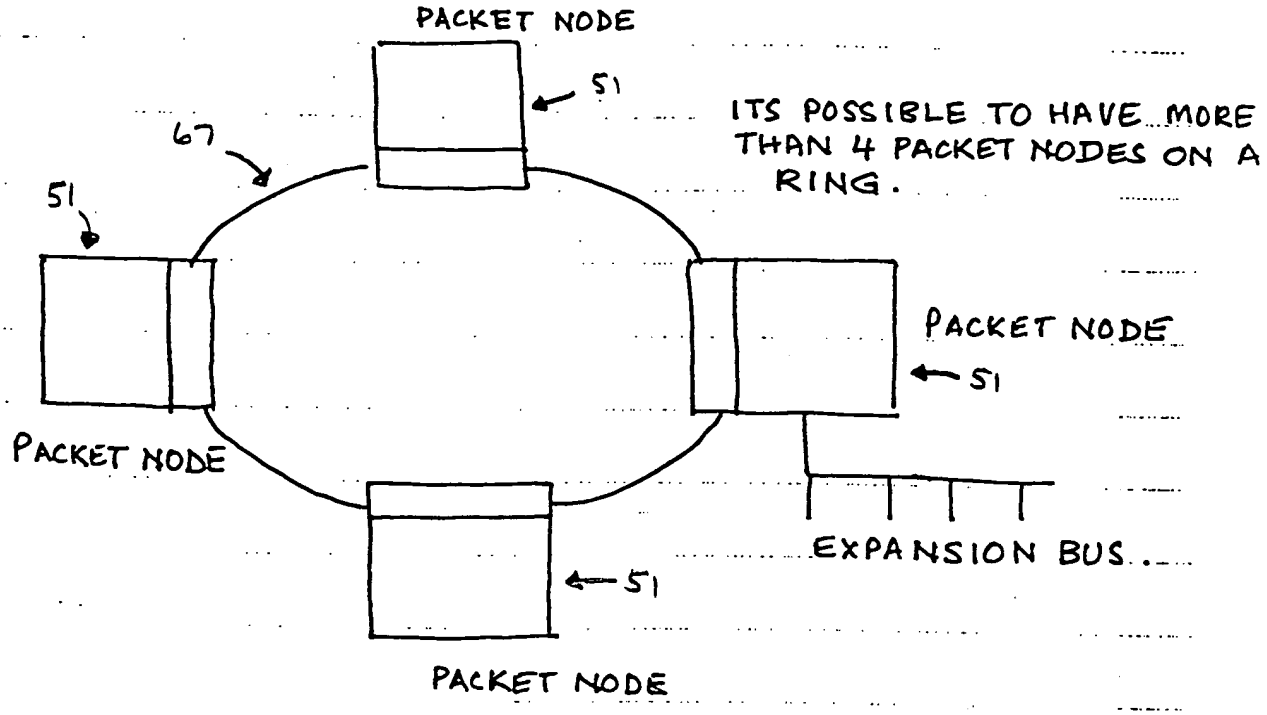
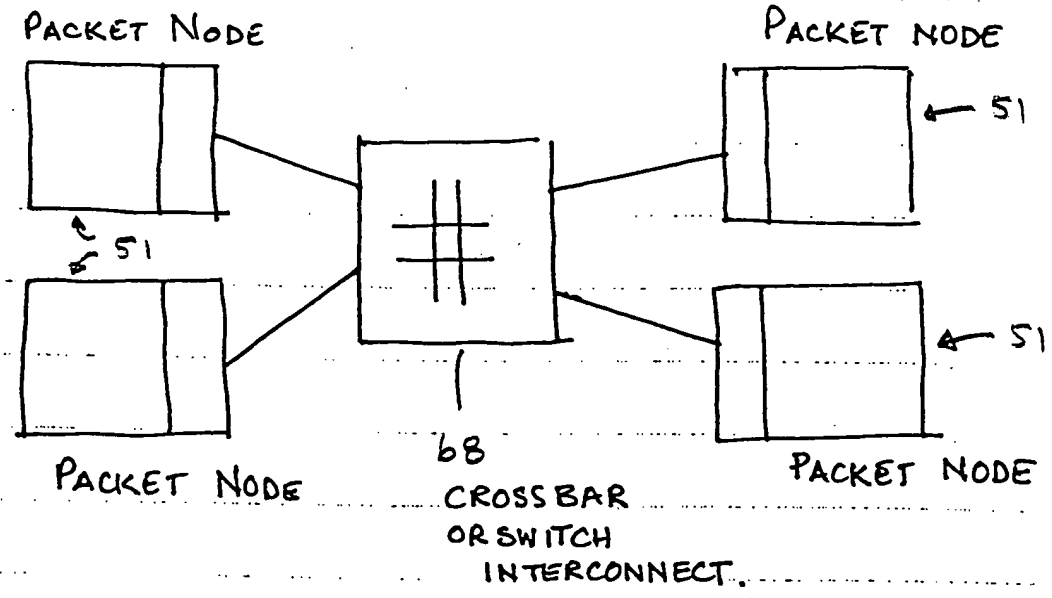


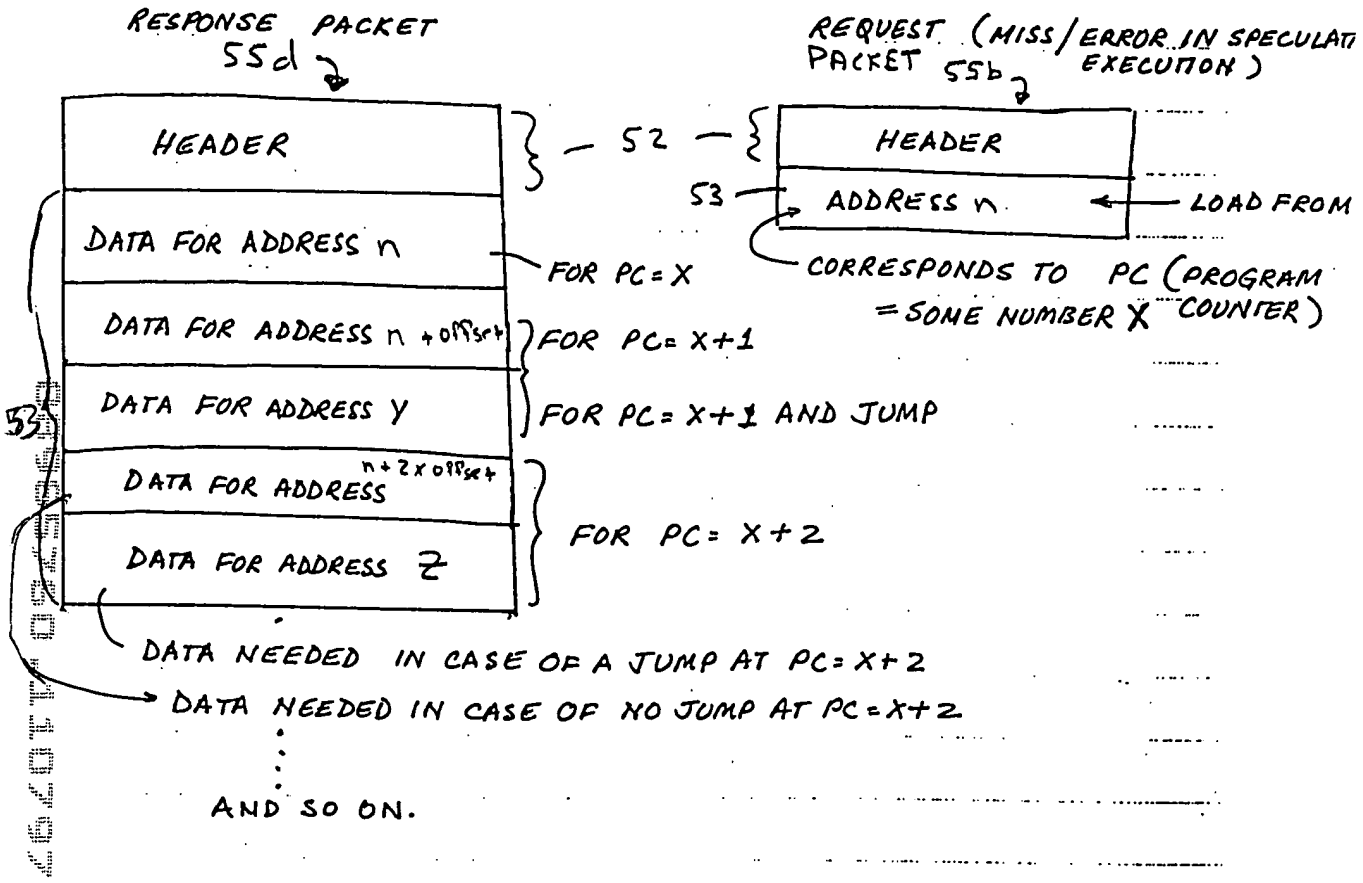
FIG. 25



Oracle-Exhibit 2015

FIG. 26.

POSSIBLE RESPONSE PACKETS FOR A REQUEST WHEN ACCESS TO TLB AND OR BTB IN THE PROCESSOR IS AVAILABLE



FOR PROGRAMS WITH VERY HIGH LOCALITY (GRAPHICS, MULTIMEDIA ETC.)

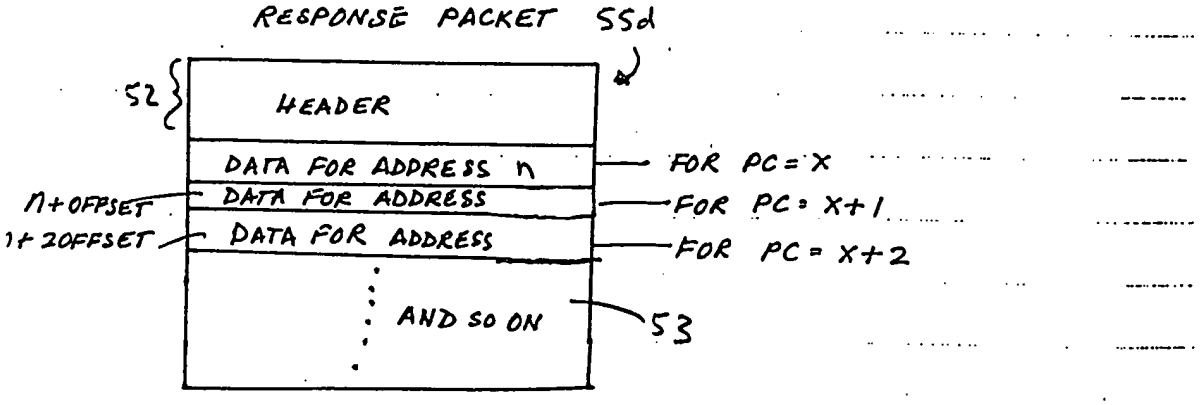


FIG. 27.

PROCESSOR NODE RECEIVE PROTOCOL

FOR PRESENT DETAILED IMPLEMENTATION THE MEMORY NOI
IS EXPECTED TO SEND ONLY THE FOLLOWING PACKETS

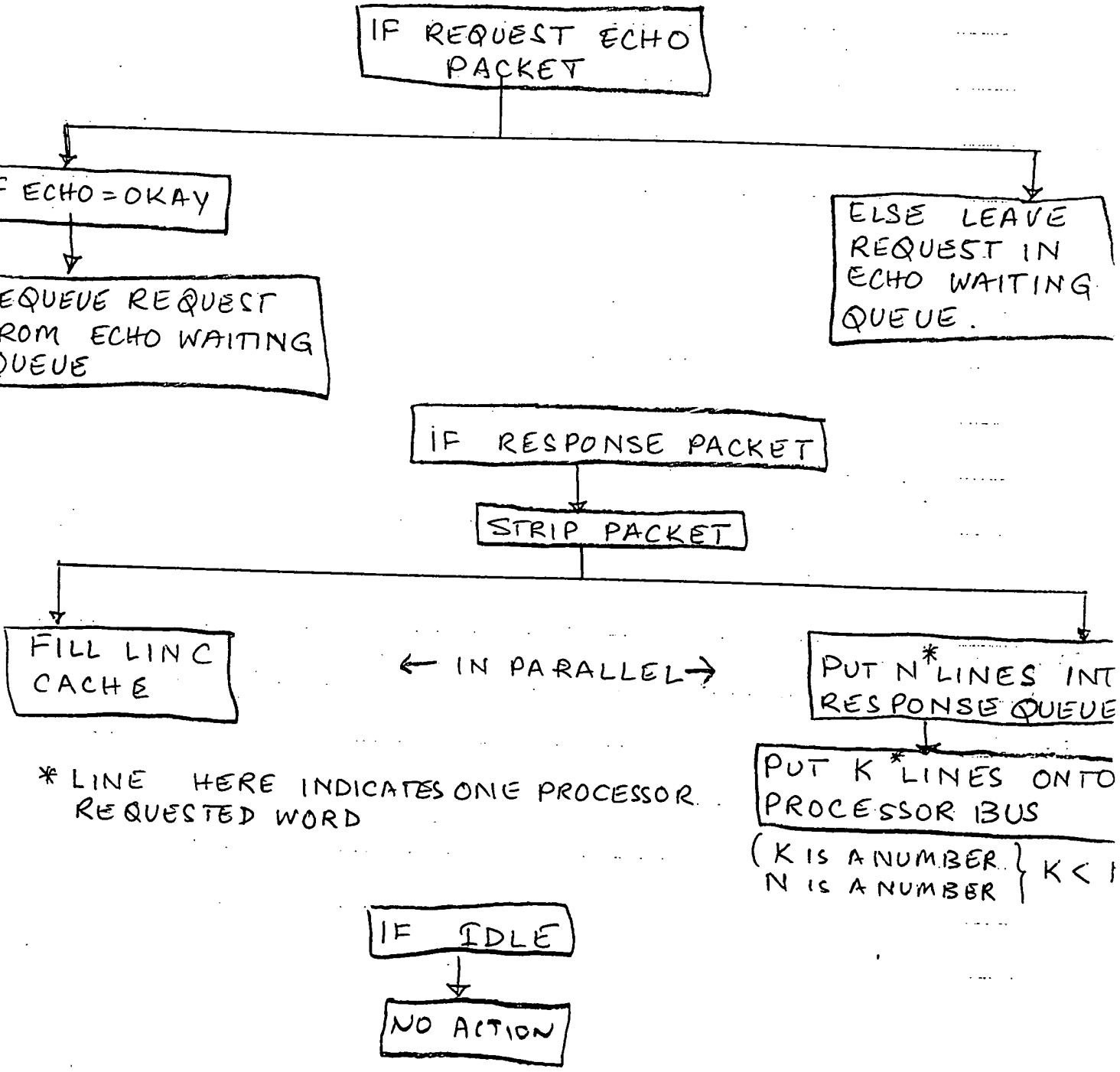
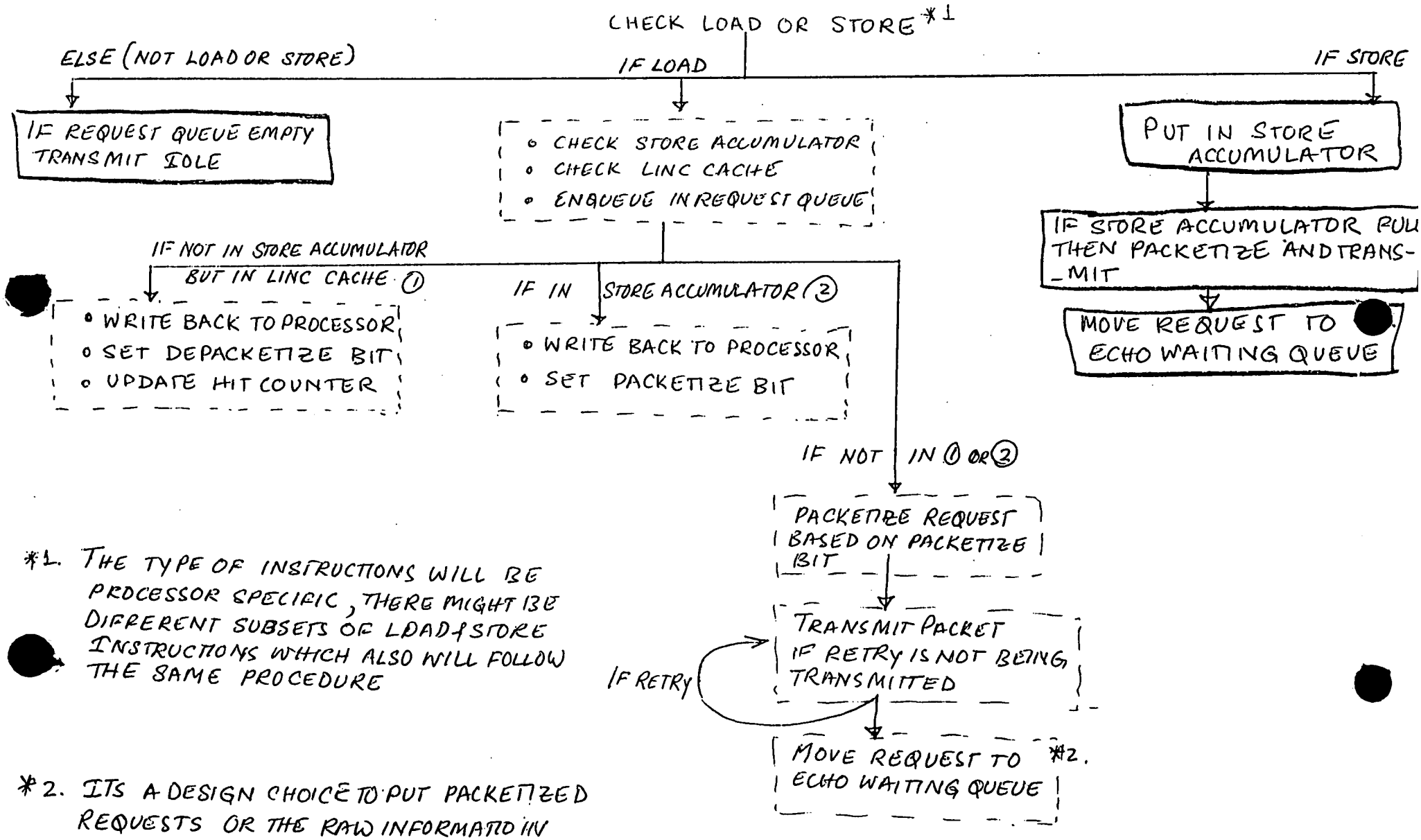


FIG. 28.

PROCESSOR NODE TRANSMIT PROTOCOL.

ALL ACTIONS WITHIN [ ] HAPPEN IN PARALLEL



*1. THE TYPE OF INSTRUCTIONS WILL BE PROCESSOR SPECIFIC, THERE MIGHT BE DIFFERENT SUBSETS OF LOAD/STORE INSTRUCTIONS WHICH ALSO WILL FOLLOW THE SAME PROCEDURE

*2. ITS A DESIGN CHOICE TO PUT PACKETIZED REQUESTS OR THE RAW INFORMATION IN THE ~~REQUEST~~ ECHO WAITING QUEUE.

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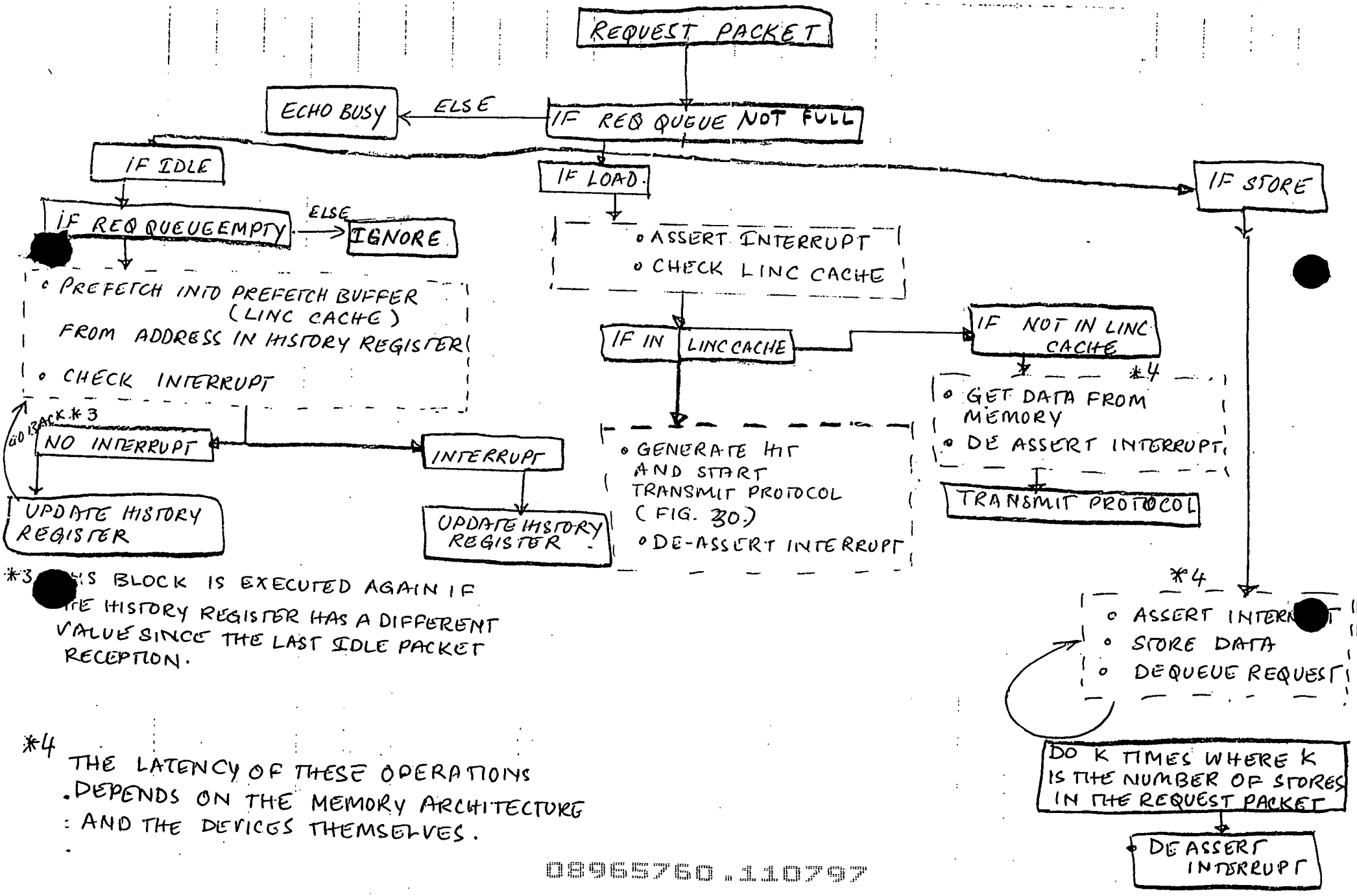
FIG. 29.

MEMORY NODE RECIEVE PROTOCOL.



*3 THIS BLOCK IS EXECUTED AGAIN IF THE HISTORY REGISTER HAS A DIFFERENT VALUE SINCE THE LAST IDLE PACKET RECEPTION.

*4 THE LATENCY OF THESE OPERATIONS DEPENDS ON THE MEMORY ARCHITECTURE AND THE DEVICES THEMSELVES.

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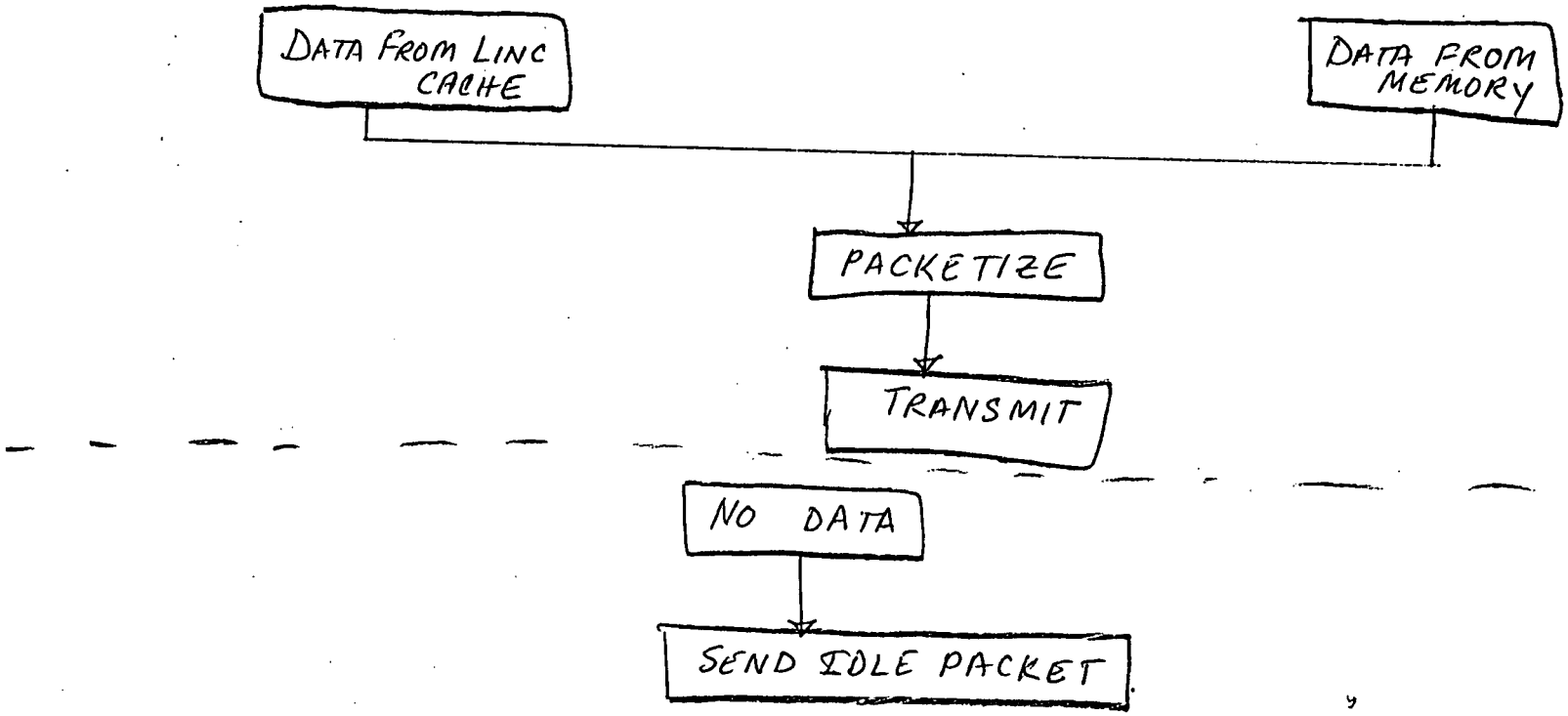
FIG. 30

MEMORY NODE TRANSMIT PROTOCOL.



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